A new large bandwidth flipped voltage follower based current mirror with low power dissipation

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Abstract

In this study, simple nMOS current mirror has been modified and the performance has been improved employing high performance flipped voltage follower (FVF). The resistively compensated FVF has been utilized at the input side of the current mirror. The advantages of using flipped voltage follower include high linearity, wide bandwidth and reduced power dissipation.

In this study, the simulation responses of all the circuits are presented. The functionality and performance improvement of all the circuits are simulated on Spectre simulator (Cadence) using model parameters of TSMC 0.18 μm CMOS BSIM 3 and level 49 technology.

Keywords: Current mirror, low power, analog circuit, cascode, voltage follower.

Introduction

The explosive growth in electronics world towards portability and high-speed VLSI systems has motivated the current research in the direction of high frequency analog basic cells. The requirement of high-performance analog devices in the communication systems has increased the usage of current-mode circuits. Current mirror is among the most important and essential current mode device that has been used in numerous analog systems.[1-9]

The important features of a current mirror include accurate current mirroring, large input and output current swings, high output impedance and good linearity. In the design of a current mirror the key issues are the improvement of high-frequency characteristic and the realization of high output impedance. Also, a current mirror which has high power consumption and small -3 dB frequency is not reliable for low-voltage high-speed applications. Several large bandwidth current mirrors are reported in literature.[1]

Gupta et al[10] have improved the frequency performance of FVF based current mirror by introducing both passive[3,4] and active resistance[3,4] at the gate of input transistor pair of the low voltage current mirror in. An approximately 200 MHz improvement in the bandwidth of passively and actively compensated current mirrors has been obtained.[10] In this work, the conventional current mirrors (CMs) have been redesigned for high frequency applications.

Simple Current Mirror

Voo and Toumazou[3] have improved the bandwidth of the simple current mirrors by using resistive compensation technique. They have introduced a compensating resistor in between the drain and gate of the input MOS transistor of the current mirror. This leads to introduction of one-pole and one-zero in the transfer function and the zero is used to cancel the dominant pole (pole-zero cancellation). Hence, the bandwidth of the system will get increased.[3] A simple CM consists of 2 MOS transistors with compensating resistor R as shown in fig. 1.

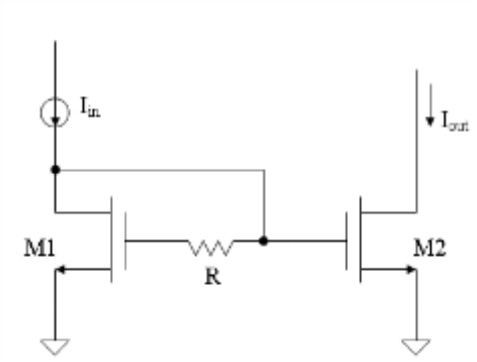

Fig. 1: Simple CM [3]

The transfer function (TF) of the current mirror without compensating resistor R[3] is:

$$A_i(s) = \frac{g_{m2}}{g_{m1}} \frac{1}{\left(1 + s\left(2C_{gs}/g_{m1}\right)\right)}$$ and bandwidth is:

$$\omega_0 = \left(\frac{g_{m1}}{2C_{gs}}\right)$$

where g_m is the transconductance and C_{gs} is the gate-source capacitance of each MOS transistor. With compensating resistor, TF of the current mirror is transformed:

$$A_i(s) = \frac{g_{m2}}{C_{gs2}} \frac{\left(s + 1/RC_{gs1}\right)}{\left(s^2 + \left(\frac{C_{gs1} + C_{gs2}}{RC_{gs1}C_{gs2}}\right)s + \left(\frac{g_{m1}}{RC_{gs1}C_{gs2}}\right)\right)} \quad (1)$$

The transfer function of the simple current mirror is transformed from first order single pole to second order low pass consisting of 1 zero and 2 poles. The zero and poles of the resistively compensated simple current mirror are:

$$Z_1 = -\frac{1}{RC_{gs1}} \quad \text{and}$$

$$P_{1,2} = \frac{C_{gs1}+C_{gs2}}{2RC_{gs1}C_{gs2}}\left[-1 \pm \sqrt{1-\frac{4g_{m1}RC_{gs1}C_{gs2}}{\left(C_{gs1}+C_{gs2}\right)^2}}\right] \quad (2)$$

From equation (1), the bandwidth of the system is obtained as (3):

$$\omega_0 = \sqrt{\frac{g_{m1}}{RC_{gs1}C_{gs2}}} \quad (3)$$

For $R = 1/g_{m1}$ and $C_{gs1} = C_{gs2}$, the zero gets cancelled with one of the poles resulting into a first order transfer function. The -3 dB frequency of the compensated CM[3] is: $\omega_0 = \left(\frac{g_{m1}}{C_{gs}}\right)$. It can be concluded that the -3 dB frequency of the resistively compensated CM is twice that of the previous one. Same method has been further applied for bandwidth increment of a FVF based cascode current mirror.

The conventional LVCCM

The conventional simple current mirror structure has drawbacks of low ratio of output to input impedance. Some circuits were reported earlier such as regular cascode current mirrors to improve the output impedance but suffer from increased minimum supply voltage which limited the applicability of these structures for low voltage operation.[11-14] In order to meet the present electronics industry requirements of low power supply, many circuits are available and the most commonly used cell is the FVF based LVCCM.[1,15-19] It can is seen that the performance of FVF based cascode current-mirrors (shown in fig. 2) including maximum operating signal and error of current transfer, is better in comparison to conventional LVCCM.

Thus, FVF based CMs could be used in good-performance and low operating voltage analog systems. If all transistors of the current mirror are in the saturation region, shunt feedback causes impedance at input node to be low. Thus, the current flow amount through this input node will not affect its voltage. Hence designer can achieve high performance current mirror.[10] Another CM topology which is extensively used in analog application is alternatively-fed FVF based cascode current mirror[1] as depicted in fig. 3.

The minimum required supply voltage (V_{DD}) and minimum output voltages (V_{out}) are expressed:[1,20]

$$V_{DD,\min} = V_{TH(Mn11)} + V_{DS,sat(Mp1)} \quad (4)$$

$$V_{in,\min} = V_{TH(Mn11)} + V_{DS(Mn5)} \quad (5)$$

$$V_{out,min} = V_{DS,sat(Mn2)} + V_{DS,sat(Mn3)} \quad (6)$$

In order to further decrement of the input resistance (R_{in}), the topology of FVF based cascode CM is modified in a way that input current is fed at a different node i.e. output node of the input FVF [1]. The minimum required V_{DD} and minimum V_{out} are obtained as: [1,20]

$V_{DD,min} = V_{TH(Mn1)} + V_{DS,sat(Mp1)}$ and $V_{in,\min} = V_{DS,sat(Mn11)}$.

It can be noticed from equations (9) and (12) that there is a significant reduction in input voltage. The Rin of the FVF based cascode CM is given by the expression:

$$R_{in} \cong \frac{2}{g_{m1}g_{m5}r_{o5}}$$

where gmi (i=1, 5) is the transconductance of Mi and r_{o5} is the output impedance of the M5 transistor.

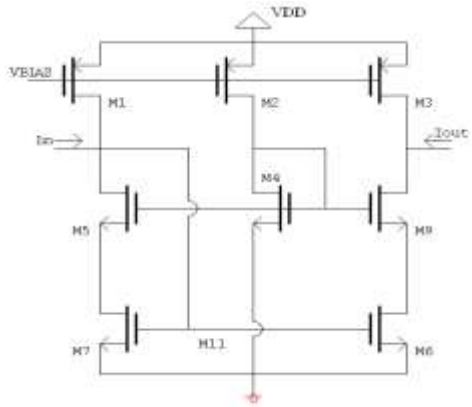

Fig. 2: FVF based LVCCM[1]

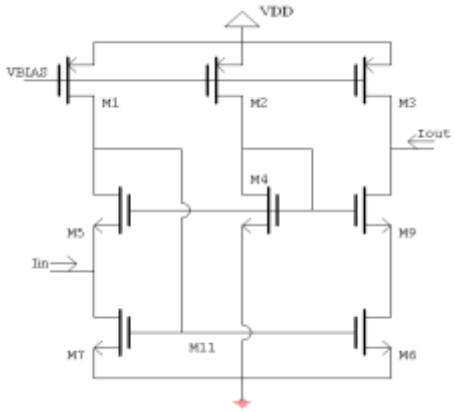

Fig. 3: Alternatively fed FVF based LVCCM

Resistively compensated FVF based LVCCM

The resistively compensated low voltage FVF based CM has been designed. The wideband flipped voltage follower has been inserted at the input terminal of the LVCCM shown in fig. 4 to enhance the bandwidth of the circuit.[10] The modified CM is shown in fig. 5 (R_{COMP} and R are compensating and feedback resistance respectively). Fig. 6 shows the actively compensated CM suggested by Gupta et al[10] and the modified version of fig. 6 is shown in fig. 7 (M_{COMP} is the transistor used for active compensation).

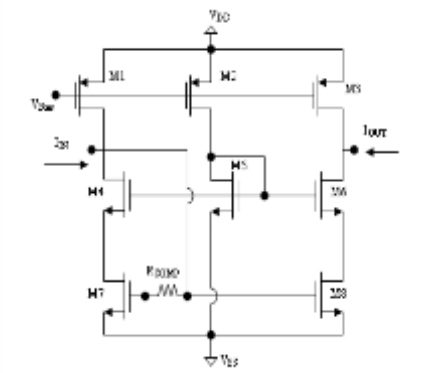

Fig. 4: Passively compensated CM[10]

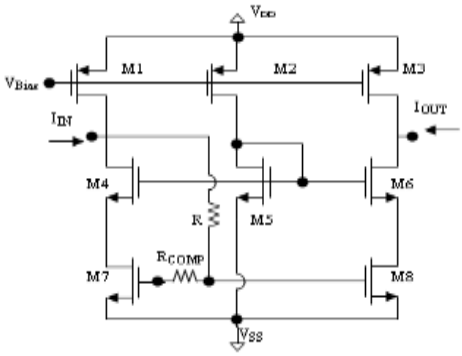

Fig. 5: Modified CM with the resistively compensated FVF

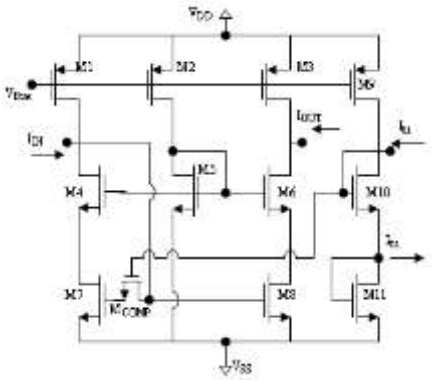

Fig. 6: Actively compensated CM[10]

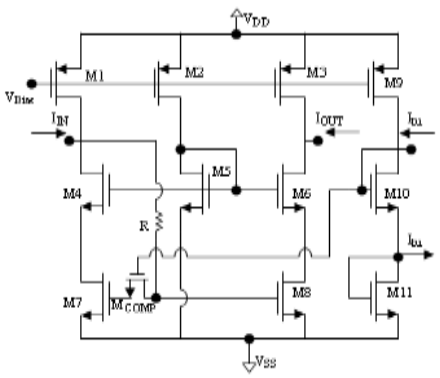

Fig. 7: Modified actively compensated CM with the resistively compensated FVF

Simulation Results and Discussion

Spectre simulator of Cadence using model parameters of TSMC 0.18 μm CMOS BSIM 3 and level 49 technology has been used to authenticate the functionality and performance development of all analog circuits. The simulation results of all the compensated LVCCMs are shown here.

The error (Iout-Iin) is shown in fig. 8 and it is almost -3.37%. The input and output compliances are portrayed in figures 9 and 10 respectively. From fig. 11, it can be seen that at 50 μA input current the modified CM dissipates 324.3 μW. It can be seen that when CM circuits are modified, the DC performance factors do not vary. Fig. 12 and 13 show the effect of resistive compensation on both the resistances of CMs. The obtained input and output resistances of CMs are 1.935 kΩ and 0.22 MΩ respectively. It can be observed from fig. 12 that the Rin of the CM decreases with frequency as the value of feedback resistance R increases (conventional CM is shown by solid line, CM with R = 1.6 kΩ and 6 kΩ are shown by dotted line with cross marker and dashed line with circle marker respectively).

Therefore, it leads to enhanced current flow at node output of FVF and input node of CM. From fig. 13, it can be seen that the output resistance of the designed LVCCM is same. Fig. 14 shows the frequency responses of CMs (fig. 2 and fig. 4 and 5). An improvement of 1.2 GHz in -3dB frequency is achieved by using the wideband FVF in passively compensated CM[10] i.e. BWER is 1.3 approximately.

However, peaking has been observed to achieve BWER of 1.6 which limits the maximum value of the compensating resistor. The frequency responses of the conventional and modified (fig. 6 and 7) actively compensated CMs can be depicted in fig. 14. The BWER is 1.2 of the improved actively compensated CM. It can be seen from figures 14 and 15 that the bandwidths of the passively compensated CMs are larger than that of the actively compensated CM. Active implementation of the compensating resistor provides several advantages such as smaller chip area requirement, but it provides smaller bandwidth than a passive resistor and increases peaking in the frequency response.

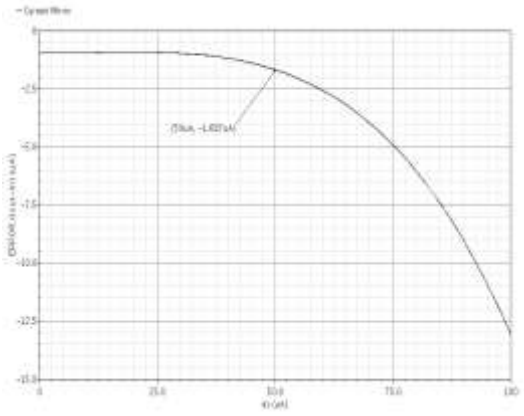

Fig. 8: Transfer error (Iout-Iin)

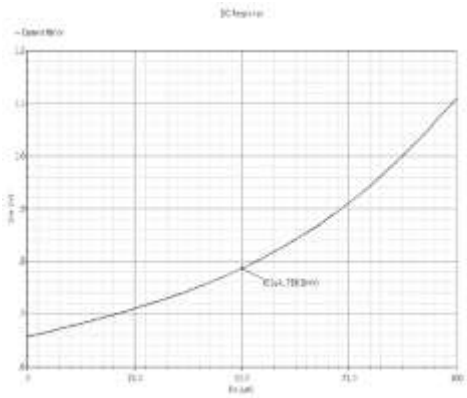

Fig. 9: Input Voltage (Vin) Versus Input Current (Iin)

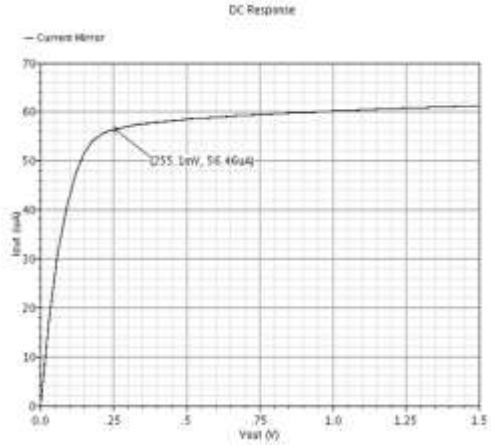

Fig. 10: Output Current (Iout) as a function of Vout

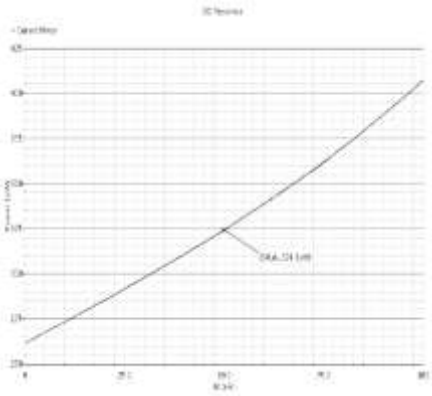

Fig. 11: DC power consumption

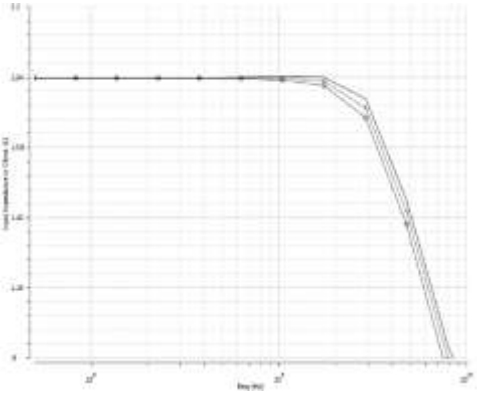

Fig. 12: Rin of (Fig. 2) and (Fig. 4 and 5) CMs

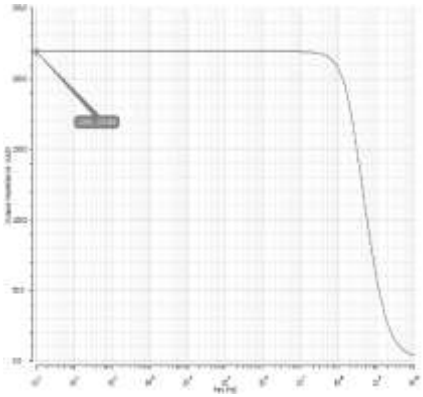

Fig. 13: Output impedance w.r.t frequency

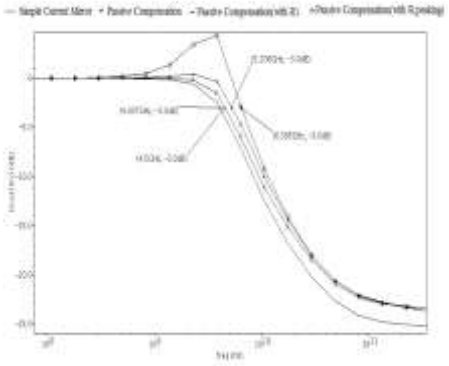

Fig. 14: Frequency responses of passively compensated CM (Fig. 5)

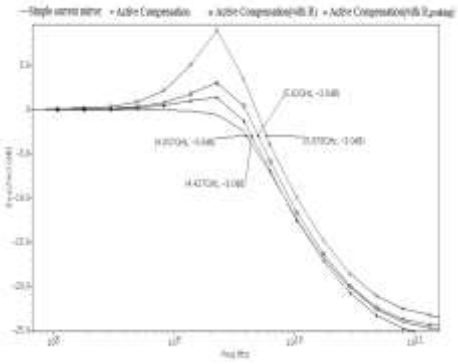

Fig. 15: Frequency responses of actively compensated CM (Fig. 7)

Conclusion

This work is dedicated to the development of FVF based conventional CM with lower power consumption. A resistively compensated FVF is used in place of conventional one in the low voltage CM to increase the -3dB frequency. The bandwidth of the proposed wideband passively compensated and actively compensated CMs is 6.395 GHz and 5.02 GHz respectively. From simulation results it has been inferred that the designed CMs circuits exhibit large bandwidth without any variation in the DC performances and hence, these circuits may find wide range of applications in high speed signal processing systems.

References

1. Koliopoulos C. and Psychalinos C., A Comparative study of the performance of the flipped voltage follower based low voltage current mirror, IEEE Int. Symp. Circuits and Systems, 1-4 **(2007)**

2. Carvajal R., Ramirez-Angulo J., Lopez Martin A., Torralba A., Galan J., Carlosena A. and Chavero F., The Flipped voltage follower: a useful cell for low voltage low power circuit design, *IEEE Trans. on Circuits and Systems*, **52(7)**, 1276 – 1279 **(2005)**

3. Voo T. and Toumazou C., High-speed current mirror resistive compensation technique, *IEE Electronics Letters*, **31(4)**, 248 – 250 **(1995)**

4. Voo T. and Toumazou C., Precision temperature stabilised tunable CMOS current-mirror for filter applications, *IEE Electronics Letters*, **32(2)**, 105-106 **(1996)**

5. Voo T. and Toumazou C., Efficient tunable continuous-time integrated current-mode filter designs, IEEE International Symposium on Circuits and Systems, 93-96 **(1996)**

6. Rajput S.S. and Jamuar S.S., A high performance current mirror for low voltage design. IEEE Circuits and Systems, In proc IEEE APCCAS, Tianjin, China 170-173 **(2000)**

7. Rajput S.S. and Jamuar S.S., Advanced current mirrors for low voltage analog designs, Proc. of IEEE ICSE '04, Kuala Lumpur, Malaysia, 258-263 **(2004)**

8. Rajput S.S. and Jamuar S.S., Low voltage, low power, high performance current mirror for portable analogue and mixed mode applications. Circuits, Devices and Systems, IEE Proc., 273 – 278 **(2001)**

9. Jamuar S.S. and Rajput S.S., Low-voltage current-mode analog circuit structures and their applications, IEEE International ASIC/SOC Conf., 477- 478 **(2002)**

10. Gupta M., Aggarwal P., Singh P. and Jindal N.K., Low voltage current mirrors with enhanced bandwidth, *Analog Integrated Circuits Signal Process*, **59**, 97-103 **(2009)**

11. Prodanov V. and Green M., CMOS current mirrors with reduced input and output voltage requirements, *IEE Electronic Letters*, **32(2)**, 104-105 **(1996)**

12. Ledesma F., Garcia R. and Ramirez-Angulo J., Comparison of new and conventional low voltage current mirrors, Midwest Symp. on Circuits and Systems, 49-52 **(2002)**

13. Yonghua C. and Geiger R.L., Cascode current mirrors with low input, output and supply voltage requirements, IEEE Midwest Symp. on Circuits and Systems, 490 – 493 **(2000)**

14. Palumbo G., On the high-frequency response of CMOS cascode current mirror, IEEE proc., 7th Mediterranean Electrotechnical Conf., 1211-1214 **(1994)**

15. Ramirez-Angulo J., Gupta S., Padilla I., Carvajal R.G., Torralba A., Jimenez M. and Munoz F., Comparison of conventional and new flipped voltage structures with increased input/output signal swing and current sourcing/sinking capabilities, *Midwest Symposium on Circuits and Systems*, 1151-1154 **(2005)**

16. Ramirez-Angulo J., Carvajal R.G., Torralba A. and Galan J., Low supply voltage high-performance CMOS current mirror with low input and output voltage requirements, *IEEE Trans. on Circuits and Systems-II*, **51(3)**, 124-129 **(2004)**

17. Meaamar A., Low-Voltage, High-Performance Current Mirror Circuit Techniques, IEEE International Conf. on Semiconductor Devices, Kuala Lumpur, Malaysia, 661-665 **(2006)**

18. Torralba A., Carvajal R.G., Ramirez-Angulo J. and Munoz E., Output stage for low supply voltage, high-performance CMOS current mirrors, *Electronics Letters*, **38(24)**, 1528 – 1529 **(2002)**

19. Aggarwal B., Gupta M. and Gupta A.K., A comparative study of various current mirror configurations: Topologies and characteristics, *Microelectronics Journal*, **53**, 134-155 **(2016)**

20. Razavi B., Design of Analog CMOS Integrated Circuits, McGraw-Hill, Inc. **(2001)**.

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